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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,553	07/07/2003	Edouard D. de Fresart	SC11342ZP C01	5864

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FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,553	DE FRESART ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *44* is/are allowed.

6)☒ Claim(s) *34-43,45,48-51,53,55-64* is/are rejected.

7)☒ Claim(s) *46,47,52 and 54* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 34-40, 42, 45, 48-50, 51, 53, 55, 56, and 57-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tung (U.S. Pat. 6,110,803) in view of Kitamura et al. (U.S. Pat. 5,844,275), all of record.

With reference to the figure drawing 2F, Tung teaches a method of manufacturing a semiconductor component comprising the steps of:

providing a p-type substrate (200) having a surface;

forming by a LOCal Oxidation of Silicon (LOCOS) process a non-electrically conductive region (228) substantially located below a substantially planar plane defined by the surface of the substrate;

forming a drift region (250) in the substrate;

forming a channel region (221) in the substrate, at least a portion of the drift region (250) located between the channel region (221) and the non-electrically conductive region (228); and forming an electrically floating regions (219) in the substrate and contiguous with the non-electrically conductive region.

Note that p-type regions (219) are electrically floating regions because the regions 219 are not connected to any power source.

Tung differs from the claims in that while Tung forms the non-electrically conductive region (228) by LOCOS process, the claims call for a non-LOCOS process to form the same.

Kitamura et al. teach an advantage of a trench isolation over the conventional LOCOS isolation (Figs. 3A-3B and col. 6, lines 1-6; col. 9, lines 10-16; col. 10, lines 3-18).

It would have been obvious to one of ordinary skill in the art to modify Tung's process by forming the non-electrically conductive region (228) by a trench isolation process as suggested by Kitamura et al. because of the advantages mentioned in the above sections namely the withstand voltage is improved, the on-resistance and the cell pitch are reduced, thereby improving the performance of the device and increasing chip density per wafer.

For claim 34, the left most floating region 219 is located between the non-electrically conductive region 228 and the channel region 221 and it also located underneath region 228.

For claim 35, see Figs. 2A and 2B for the formation of the channel region (221) and the electrically floating regions (219) occurs simultaneously with each other.

For claims 37-39, see col. 5, line14 and col. 8, lines 21-22 for the materials of the trench fillers.

As for claim 40, the Examiner takes official notice that lining the trench walls with a thermal oxide layer before filling the trench with semi-insulating polysilicon is an old practice in the art.

For claim 42, Figs. 6 and 7 show planar trench surfaces, i.e., the trench fill materials are planarized.

For claim 51, the non-electrically conductive region 228 is located between the drain region 244 and the channel region 221; and the right most floating region 219 is located between region 228 and the drain region 244.

For claim 55, channel region (221) is electrically isolated from the substrate (202) located underneath the channel region because the channel region and the substrate have opposite type of conductivity.

For claim 56, channel region 221 includes two portions 212 and 220. The channel portion 220 is electrically coupled to a portion of the substrate (p-type region which forms pn junction with n-type layer 202) located underneath the channel portion 220).

For claim 57, the left most floating region 219 is located partially under the gate electrode 234

For claims 62 and 63, when all three p-type regions (219) are considered as a single electrically floating region, the electrically floating region comprises a first portion (e.g., the first p-type region (219)) and the second portion (e.g., the second p-type region (219)), and the first portion is separate from the second portion as shown in Fig. 2F.

2. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tung taken with Kitamura et al. as applied to claims 34-40, 42, 45, 48-50, 51, 53, 55, 56, and 57-64 above, and further in view of Yasuhara et al. of record.

The combination of Tung and Kitamura et al. teaches a process as mentioned above. The combined process differs from the claims in not disclosing the claimed step of implanting a dose of oxygen into the surface of the substrate at location corresponding to the non-electrically conductive region. However, Yasuhara et al.

in col. 5, lines 28-29 suggest that "The resistance of the film 14 can be adjusted by the concentration of oxygen contained therein..." Thus, one skilled in the art would recognize that incorporating oxygen into the SIPOS film would increase the resistance of the film because oxygen atoms would react with silicon atoms in the SIPOS to form silicon oxide that possesses insulation property. Therefore, in the case where the trench is filled with a semi-insulating polysilicon (SIPOS) as taught in Kitamura, it would have been obvious to one having ordinary skill in the art to incorporate oxygen into SIPOS film because this would increase the resistance of the SIPOS film, hence increasing the isolation property of the trench. Moreover, introducing oxygen atoms into a region by implantation is well known in the art. Thus, the limitation regarding implanting a dose of oxygen into the surface of the substrate at location corresponding to non-electrically conductive region (i.e., trench isolation region) is meet.

3. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tung taken with Kitamura et al. as applied to claims 34-40, 42, 45, 48-50, 51, 53, 55, 56, and 57-64 above, and further in view of Ishikawa (U.S. Pat. 6,277,706) of record.

The combination of Tung and Kitamura et al. teaches a process as mentioned above. The combined process differs from the claims in not disclosing the claimed limitation of densifying the trench fill material. However, Ishikawa teaches that densifying an oxide filled in the trench would eliminate pits, which would have caused by subsequent planarizing process (col. 5, lines 14-19, lines 32-40). Thus, in the case where the trench is filled with an oxide as taught in Kitamura, it would have been obvious to one having ordinary skill in the art to densify the filled oxide as suggested by Ishikawa because this would eliminate pits hence improves reliability of the device.

Allowable Subject Matter

4. Claim 44 is allowed over prior art of record.

5. Claims 46, 47, 52, and 54 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: claims 44, 46, 47, 52, and 54 are indicated allowable over prior art of record because the prior art does not teach or suggest the claimed feature regarding the electrically floating region are located at the surface of the substrate.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

04/15/05